REMARKS

Claims 1-30 are pending in this application. Claims 1-5, 9-11, 14-25 and 28 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over U.S. Patent Application Pub. No. 2004/0117510 ("Arimilli") in view of U.S. Patent No. 4,663,706 ("Allen"). Claims 7, 26, 27 and 30 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Arimilli and Allen in view of U.S. Patent No. 6,938,094 ("Keller"). Claims 6, 8, 12, 13 and 29 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Arimilli and Allen in view of U.S. Patent No. 6,158,014 ("Henson"). These rejections are respectfully traversed, for reasons including those set forth below.

Applicants' attorney was unable to schedule a telephonic interview with the Examiner prior to filing this response. Therefore, Applicants' attorney requests that the Examiner contact him at 510.663.1100 after considering the points raised in this response.

Independent Claims 1, 19, 22 and 28

The Office Action asserts that all independent claims are obvious over Arimilli in view of Allen. Apart from the issue of whether one of skill in the art would have been motivated to combine Arimilli and Allen (which Applicants do not concede), the resulting "Arimilli-Allen" does not teach, suggest or indicate several recitations of independent claims 1, 19, 22 and 28. Some such recitations involve point-to-point intra-cluster links. For example, claim 1 recites an interconnection controller, comprising:

> an intra-cluster interface *configured for coupling with intra-cluster links to a plurality of local nodes arranged in a point-to-point architecture in a local cluster,* the local nodes including local processors . . . . [Emphasis added.]

Claim 1 also recites:

> encapsulation logic *configured to receive intra-cluster packets from the local nodes via the intra-cluster links* and to encapsulate the intra-cluster packets as inter-cluster packets for transmission on the inter-cluster link . . . .

[Emphasis added.]

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Claim 19 recites a computer system, comprising:

a first cluster including a first plurality of processors and a first interconnection controller, *the first plurality of processors and the first interconnection controller interconnected by first point-to-point intra-cluster links*. . . . [Emphasis added.]

Claim 22 recites:

A computer system comprising a plurality of processor clusters *interconnected by a plurality of point-to-point inter-cluster links*, each processor cluster comprising nodes including a plurality of local processors and an interconnection controller *interconnected by a plurality of point-to-point intra-cluster links*, communications within a cluster being made via an intra-cluster protocol that uses intra-cluster packets, *wherein the interconnection controller in each cluster is operable to map locally-generated communications directed to others of the clusters to the point-to-point inter-cluster links* and to map remotely-generated communications directed to the local nodes to the point-to-point intra-cluster links, communications between clusters being made via an inter-cluster protocol that uses inter-cluster packets, an inter-cluster packet encapsulating at least one intra-cluster packet, each interconnection controller configured to generate and transmit a special packet on an inter-cluster link when the interconnection controller has no valid inter-cluster packets to send, the special packet not being stored in a transmission buffer prior to being transmitted on the inter-cluster link. [Emphasis added.]

Similarly, claim 28 recites:

A computer-implemented method for decreasing latency in a computer system comprising a plurality of clusters, *each cluster including a plurality of local nodes and an interconnection controller interconnected by point-to-point intra-cluster links, communications between the local nodes and the interconnection controller made via an intra-cluster protocol using intra-cluster*

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> *packets*, the interconnection controller of each cluster interconnected by inter-cluster links with the interconnection controller of other clusters . . . .

[Emphasis added.]

One example of a processor cluster having nodes connected by point-to-point intra-cluster links is shown in Fig. 2 of the present invention:

> Fig. 2 is a diagrammatic representation of a multiple processor cluster such as, for example, cluster 101 shown in Fig. 1A. Cluster 200 includes processors 202a-202d, one or more Basic I/O systems (BIOS) 204, a memory subsystem comprising memory banks 206a-206d, point-to-point communication links 208a-208e, and a service processor 212. The point-to-point communication links are configured to allow interconnections between processors 202a-202d, I/O switch 210, and interconnection controller 230.

(*Id.* at page 13, lines 9-14 [emphasis added].)

It is respectfully submitted that neither Arimilli nor Allen teaches point-to-point links within nodes (such as individual processors) of a cluster. With regard to these recitations in claim 1, for example, the Office Action references page 5, ¶ 41 of Arimilli (also referencing the same features in Fig. 4a), which indicates:

> *Each cluster C1-C3 contains four processor units 401-404 interconnected by a ring bus 410.* [Emphasis added.]

Similarly, the first sentence of the Abstract of Arimilli notes;

> Processor communication registers (PCRs) *contained in each processor within a multiprocessor system and interconnected by a specialized bus* provides enhanced processor communication. [Emphasis added.]

Likewise, Allen describes a multiprocessor system in which the individual processors communicate via an interprocessor bus. (*See, e.g.*, interprocessor bus 14 of Figs. 1 and 2.)

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Such bus-based communications between nodes (such as processors) in a device differ from the point-to-point communications between nodes described in the present invention, as noted in the Background section:

> A relatively new approach to the design of multi-processor systems replaces broadcast communication such as bus or ring architectures among processors with a point-to-point data transfer mechanism in which the processors communicate similarly to network nodes in a tightly-coupled computing system. That is, the processors are interconnected via a plurality of communication links and requests are transferred among the processors over the communication links according to routing tables associated with each processor. The intent is to increase the amount of information transmitted within a multi-processor platform per unit time.
>
> In some multi-processor systems, local nodes (including processors and an interconnection controller) are directly connected to each other through a plurality of point-to-point intra-cluster links to form a cluster of processors. Separate clusters of processors can be connected via point-to-point inter-cluster links. The point-to-point links significantly increase the bandwidth for coprocessing and multiprocessing functions. However, using a point-to-point architecture to connect multiple processors in a multiple cluster system presents its own problems.

(Id. at page 1, lines 10-24.)

For at least the reasons set forth above, the present invention is provided in a different context from that of the art relied upon for rejecting all of the independent claims. Accordingly, it is respectfully submitted that the art relied upon does not teach the claimed elements noted above and that all claims are allowable over the art relied upon. There are various other differences between the claimed invention and the art relied upon, but it is not necessary to elaborate upon these differences at present. Applicants' attorney reserves the right to do so at a later date, if necessary.

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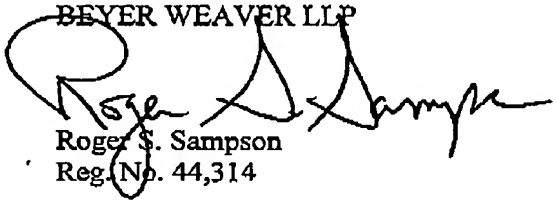
SUMMARY

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Applicant's attorney requests that the Examiner contact him by telephone at the number set out below.

The Commissioner is hereby authorized to charge any additional fees, including any extension fees, which may be required or credit any overpayment directly to the account of the undersigned, No. 50-0388 (Order No. NWISP045).

Respectfully submitted,
BEYER WEAVER LLP



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